Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTION:**

1. **1A**
2. **1B**
3. **N/C**
4. **1C**
5. **1D**
6. **1Y**
7. **GND**
8. **2Y**
9. **2A**
10. **2B**
11. **N/C**
12. **2C**
13. **2D**
14. **VCC**

**.041”**

**2 1 14 13**

**12**

**11**

**10**

**9**

**3**

**4**

**5**

**6**

**7 8**

**54LS20**

**B**

**MASK**

**REF**

**.041”**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004 x .004”**

**Backside Potential:**

**Mask Ref: 54LS20 B**

**APPROVED BY: DK DIE SIZE .041” X .041” DATE: 8/17/21**

**MFG: NATIONAL THICKNESS .015” P/N: 54LS20**

**DG 10.1.2**

#### Rev B, 7/1